MORNSUN®

SCM3406ASA Half-duplex Transceiver

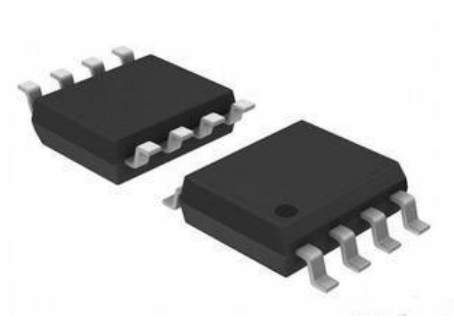
Features

- 3.0-5.5V single supply operation
- Baud Rate Up to 10Mbps
- 1/8 Unit Load—Up to 256 Nodes on a Bus
- Bus-Pin ESD Protection Up to 15kV
- Driver short circuit protection

Applications

- Industrial Automation
- Building Automation
- Smart Electricity Meter
- Remote Signal Interaction, Transmission

Package



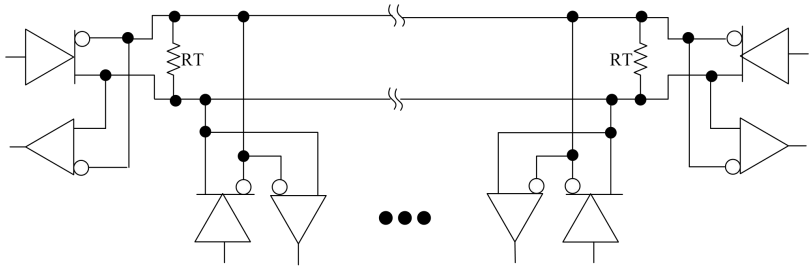
Mechanical package: SOP-8
(see “Ordering information” for details).

Functional Description

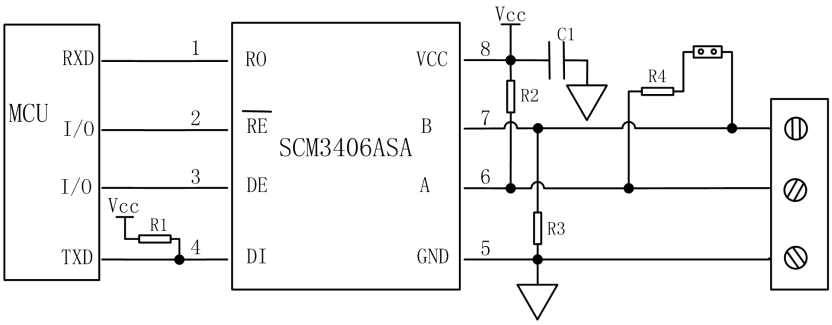
SCM3406ASA is a half-duplex enhanced transceiver designed for RS–485 data bus networks. Powered by 3VDC-5.5VDC supply, the SCM3406ASA is fully compliant with TIA/EIA-485-A standard and is suitable for data transmission of up to 10Mbps. Receivers have an exceptionally high input impedance, which places only 1/8 of the standard load on a shared bus and up to 256 transceivers .

The reliability design of A B pin is emphasized, including driver output over current protection and enhanced ESD design. The ESD protection level of A,B pin can be up to 15kV (Human Body Model).

Typical Application Circuit



Typical Circuit 1: Half-Duplex Network



Typical Circuit: 2 Application Diagram

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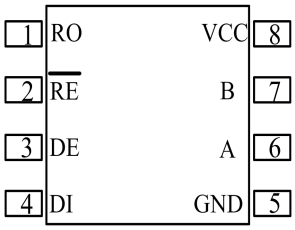
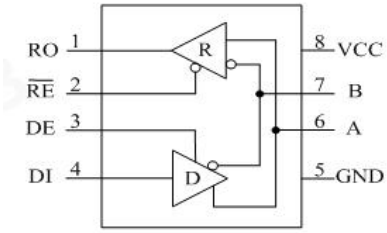
Pin Connection



Internal Block Diagram



Function table

Driver						Receiver			
Input			Outputs			Input			Output
$\overline{RE}$	DE	DI	A	B		$\overline{RE}$	DE	A-B	RO
X	H	H	H	L		L	X	≥-40mV	H
X	H	L	L	H		L	X	≤-220mV	L
L	L	X	Z	Z		L	X	Open/Short	H
H	L	X	Z (SHUTDOWN)			H	H	X	Z
						H	L	X	Z (SHUTDOWN)

Pin descriptions

Pin Number	Pin Name	Pin Functions
1	RO	Receiver Output. When $\overline{RE}$ is low and if (A – B) ≥ -40mV, RO is high. If (A – B) ≤ - 220mV, RO is low.
2	$\overline{RE}$	Receiver Output Enable. When $\overline{RE}$ is low, RO is enabled. When $\overline{RE}$ is high, RO is high impedance. Drive $\overline{RE}$ high and DE low to enter shutdown mode.
3	DE	Driver Output Enable. When DE is high, outputs are enabled. When DE is low, outputs are high impedance. Drive DE low and $\overline{RE}$ high to enter shutdown mode.
4	DI	Driver Input.
5	GND	Ground
6	A	Non-Inverting Driver Output / Receiver input
7	B	Inverting Driver Output / Receiver input
8	VCC	Positive Supply VCC. Bypass to GND with a 0.1uF capacitor.

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Absolute Maximum Ratings

General test conditions: Free-air, normal operating temperature range (unless otherwise specified).

Parameters	Unit
Supply voltage range, Vcc	-0.3V~+7V
Voltage range at A or B	-15V~+15V
Voltage range at DE、DI、$\overline{RE}$、RO	-0.3V ~ (VCC + 0.3V)
Storage Temperature	-55℃~150℃
Lead Temperature (soldering, 10s)	300℃

Support ±15V in receiver mode, and -8 ~+13V in driver mode

Important: Exposure to Absolute Maximum Rated conditions for an extended period may severely affect the device reliability, and stress levels exceeding the "Absolute Maximum Ratings" may result in permanent damage.

Recommended Operating Conditions

Recommended Operating Conditions	Min.	Typ.	Max.	Unit
Supply Voltage, V_{VCC}	3	5	5.5	V
Voltage at any bus terminal (differential or common mode), V_I	-7		12	
High-level input voltage (DI, DE, $\overline{RE}$) , V_{IH}	2		VCC	
Low-level input voltage (DI, DE, $\overline{RE}$) , V_{IL}	0		0.8	
Differential load resistance	54	60		Ω
Signaling rate			10000	kbps
Operating ambient temperature, T_A in free–air	-40		125	℃
Maximum operating junction temperature, T_J			150	℃

Electrical Characteristics

General test conditions and V_{VCC}= 5V, Ta = 25℃ (unless otherwise specified).

Parameters		Conditions		Min.	Typ.	Max.	Unit
Digital Input Signals: DI, DE, $\overline{RE}$							
Logic input thresholds		High, V_{IH}		2			V
		Low, V_{IL}				0.8	
Driver							
Differential Driver Output (V_{OD})		No Load				V_{VCC}	V
Differential Driver Output (1)		Vin=3V, R_L=54Ω, Figure16		1.5	1.9		V
Differential Driver Output (2)		Vin=5V, R_L=54Ω, Figure16		2.1	2.8		
Differential Driver Output (3)		R_L=60Ω, V_{CM} = -7 ~ 12V, VCC = 3.0~3.6V, Figure17		1.5		V_{VCC}	
Driver Common Mode Output Voltage		Figure18		1		3	V
Change in Common Mode Output Voltage		Figure19				±0.05	V
Driver Short Circuit Current Limit		-7V≤V_{OUT}≤12V, Figure22				±150	mA
Receiver							
Receiver Input Resistance		-7V≤V_{OUT}≤12V		96			kΩ
Input Current (A, B pins)		DE=0, $\overline{RE}$=0, V_{VCC}=0 or 5.5V	V_{OUT} =12V			120	uA
			V_{OUT} = -7V	-110			uA
Change in magnitude of differential output voltage		I_O = ±8 mA		-220		-40	mV
Receiver Input Hysteresis					70		mV
Receiver Output Voltage	V_{OH}, Figure 23	I_{OUT} = -8mA, Vcc = 4.5V ~ 5.5V V_{ID}= 1V		3	4.5		V
	V_{OH}, Figure 23	I_{OUT} = -8mA, Vcc = 3.0V ~ 3.6V V_{ID}= 1V		2.45	2.65		
	V_{OL}, Figure 23	I_{OUT} = 8mA, Vcc = 4.5V ~ 5.5V VID= 1V				0.4	
	V_{OL}, Figure 23	I_{OUT} = 8mA, Vcc = 3.0V ~ 3.6V VID= 1V				0.5	

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Supply and Protection						
I_{VCC}	Driver and receiver enabled	DE = V_{VCC}, $\overline{RE}$ = 0, No load		1900	2200	uA
	Driver enabled, receiver disabled	DE = V_{VCC}, $\overline{RE}$ = V_{VCC}, No load		1800	2200	uA
	Receiver enabled, driver disabled	DE = V_{VCC}, $\overline{RE}$ = 0, No load		1700	2000	uA
	Driver and receiver disabled	DE = 0, $\overline{RE}$ = V_{VCC}, No load		1650	2000	uA
ESD	Human Body Model	A, B and GND		±15		kV
		Other pins		±4		kV
	IEC61000-4-2	A, B and GND		±15		kV
EFT	IEC61000-4-4	A, B and GND		±1		kV

Transmission Characteristics

General test conditions and V_{VCC} = 5V, Ta = 25℃ (unless otherwise specified).

Parameters	Conditions	Min.	Typ.	Max.	Unit
Driver					
Data Signaling Rate	Duty Cycle 40% ~ 60%			10000	kbps
Driver Propagation Delay (T_{PHL} , T_{PLH})	R_L = 54Ω,C_L = 50pF, Figure 19		21	30	ns
Driver Output Rise/Fall Time (T_R , T_F)			8		ns
Driver Differential Skew ($\lvert T_{PHL} - T_{PLH} \rvert$)			3	6	ns
Driver Enable to Output High (T_{PZH})	R_L=110Ω, $\overline{RE}$ = 0,Figure 20, Figure 21		20	45	ns
Driver Enable to Output Low (T_{PZL})			30	50	ns
Driver Disable from Output High (T_{PHZ})			30	50	ns
Driver Disable from Output Low (T_{PLZ})			30	50	ns
Receiver					
Receiver Propagation Delay (T_{PLH} , T_{PHL})	C_L = 15pF, Figure 22		35	50	ns
Receiver Differential Skew ($\lvert T_{PLH} - T_{PHL} \rvert$)			10	15	ns
Receiver Output Rise/Fall Time (T_R , T_F)	C_L = 15pF, V_{DI}=-1.5V~1.5V, Figure 22		14		ns
Receiver Enable to Output High (T_{PZH})	C_L = 15pF, Figure 23, Figure 24		20	30	ns
Receiver Enable to Output Low (T_{PZL})			25	40	ns
Receiver Disable from Output High (T_{PHZ})			30	60	ns
Receiver Disable from Output Low (T_{PLZ})			30	60	ns

Typical Performance Curves

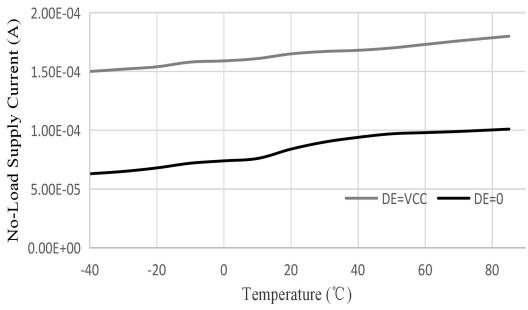

Figure 1 No-Load Supply Current vs. Temperature

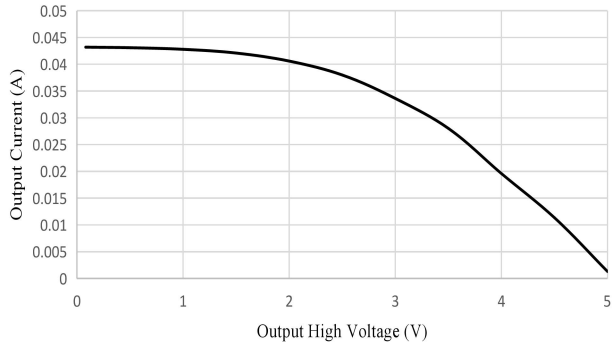

Figure 2 Output Current vs. Receiver Output High Voltage

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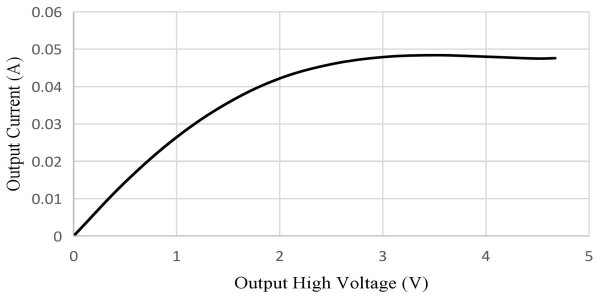

Figure 3 Output Current vs. Receiver Output Low Voltage

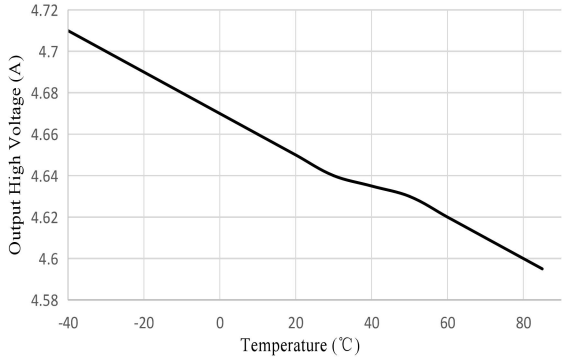

Figure 4 Receiver Output High Voltage vs. Temperature

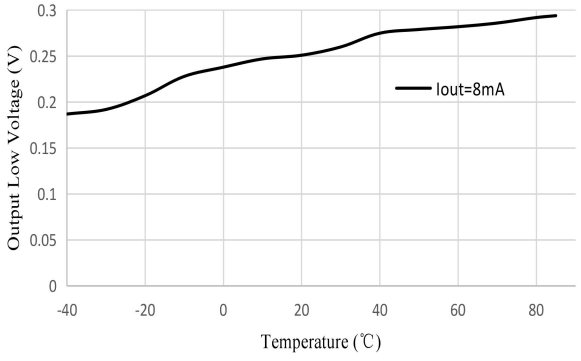

Figure 5 Receiver output low voltage vs. Temperature

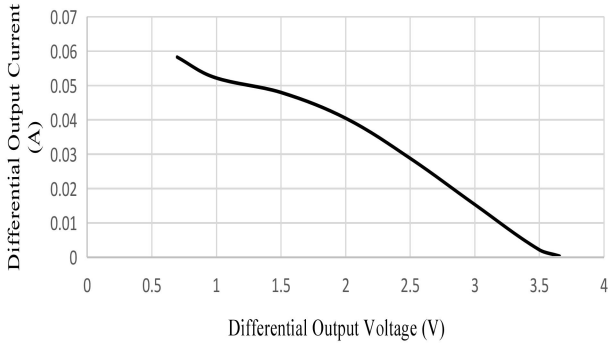

Figure 6 Driver differential output current vs. Differential output voltage

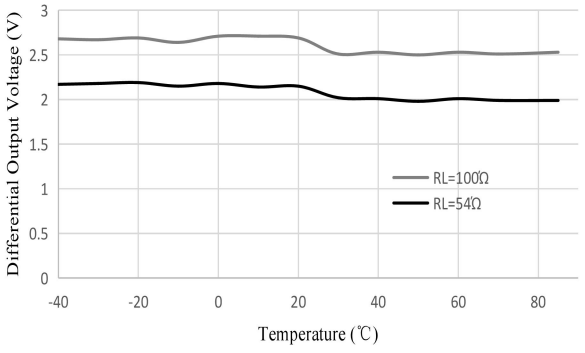

Figure 7 Driver Differential Output Voltage vs Temperature

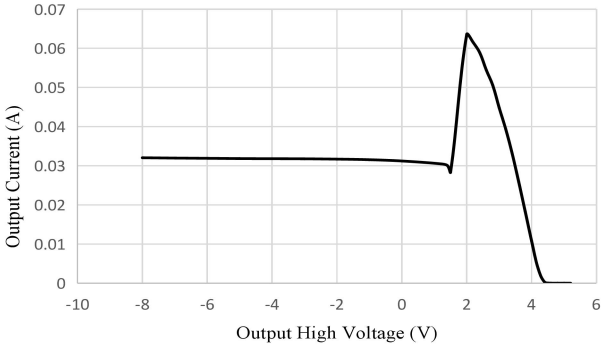

Figure 8 Output current vs. Transmitter output high voltage

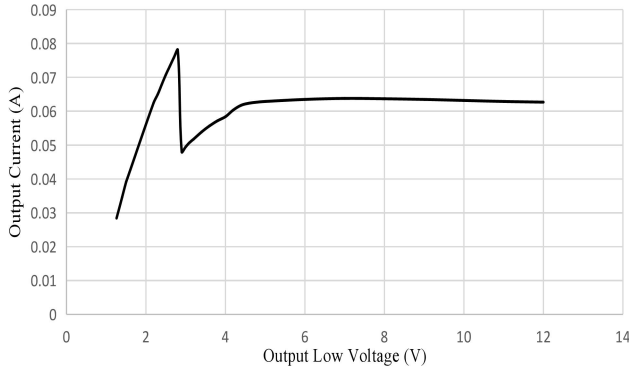

Figure 9 Output current vs. Transmitter output low voltage

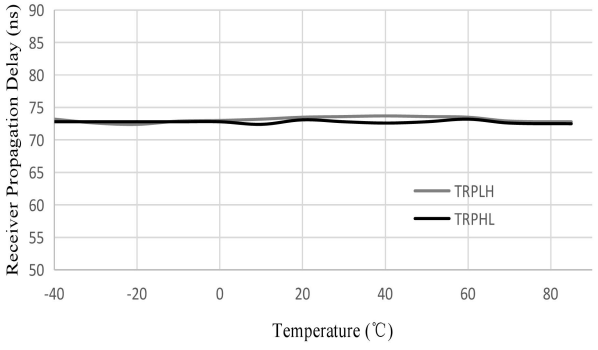

Figure 10 Receiver Propagation Delay vs. Temperature

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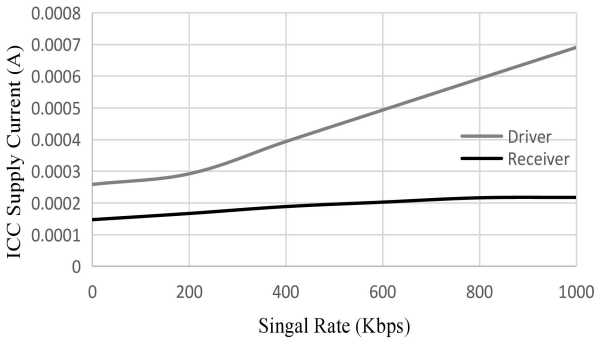

Figure 11 RMS Supply Current vs. Signaling Rate

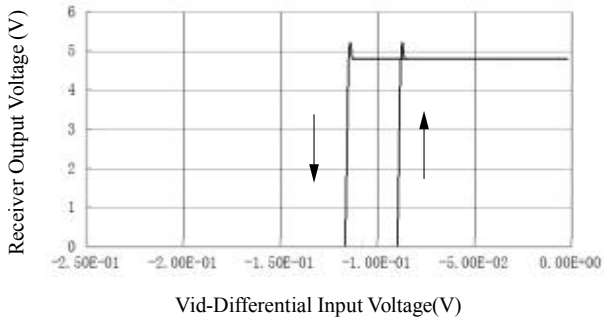

Figure 12 Receiver output voltage vs. Differential input voltage

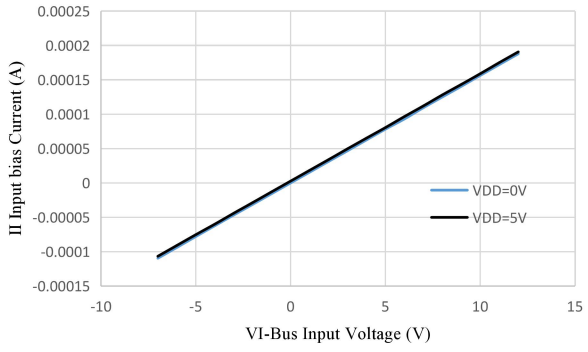

Figure 13 Bus input current vs. Bus input voltage

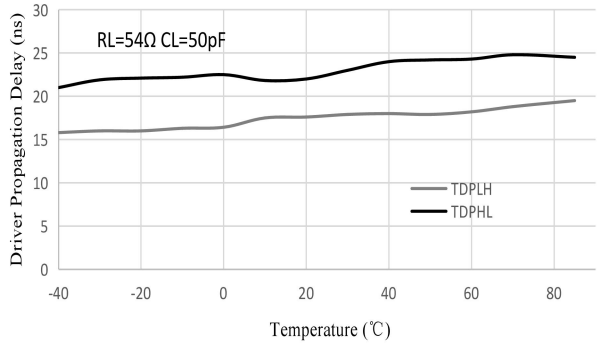

Figure 14 Driver propagation delay vs. Temperature

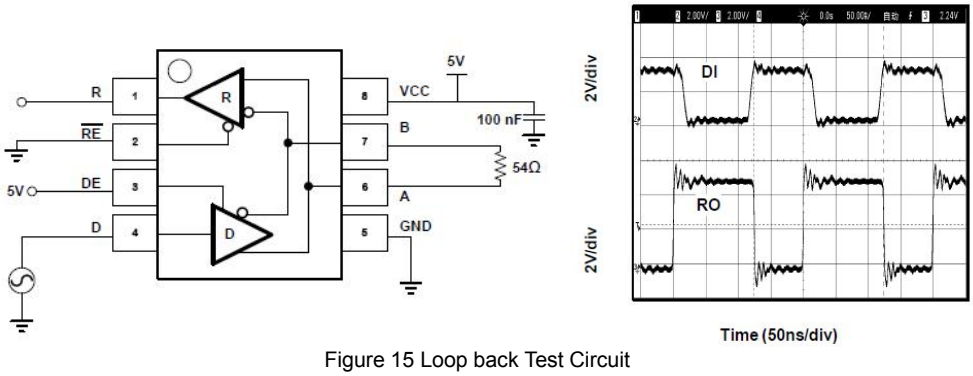

Figure 15 Loop back Test Circuit

Test Circuits

Note: Load test capacitance includes probe and test fixture stray capacitance, unless otherwise specified. Signal generator with following characteristics: Rise and fall time < 6ns, pulse rate 100kHz, 50% duty cycle, ZO = 50Ω (unless otherwise specified).

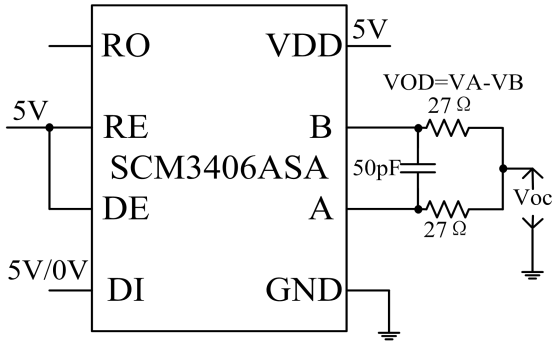

Figure 16 Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

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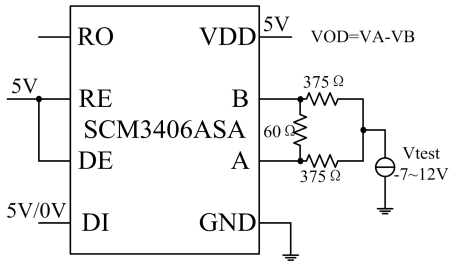

Figure 17 Driver Test Circuit, V_{OD} With Common-Mode Loading

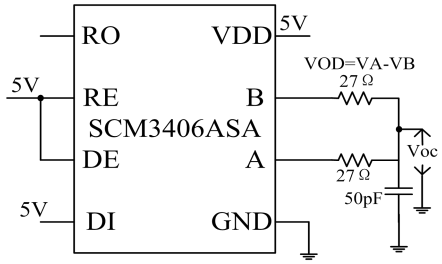

Figure 18 Driver V_{OC} Test Circuit

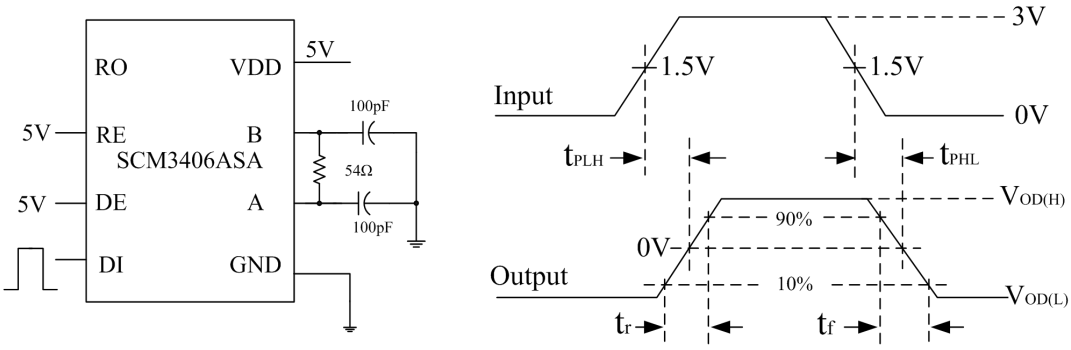

Figure 19 Driver Switching Test Circuit and Waveforms

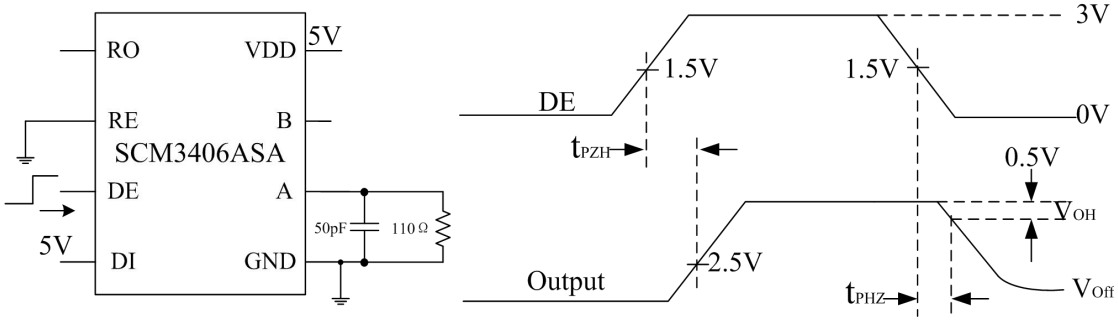

Figure 20 Driver Enable/Disable Test Circuit and Waveforms, High Output

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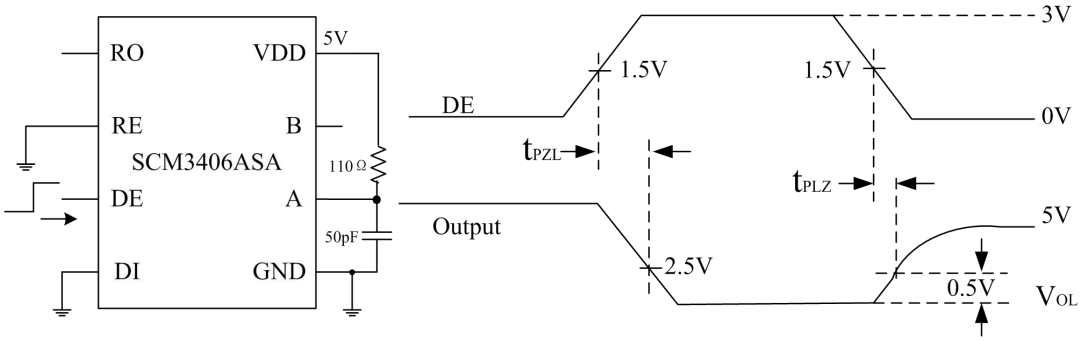

Figure 21 Driver Enable/Disable Test Circuit and Waveforms, Low Output

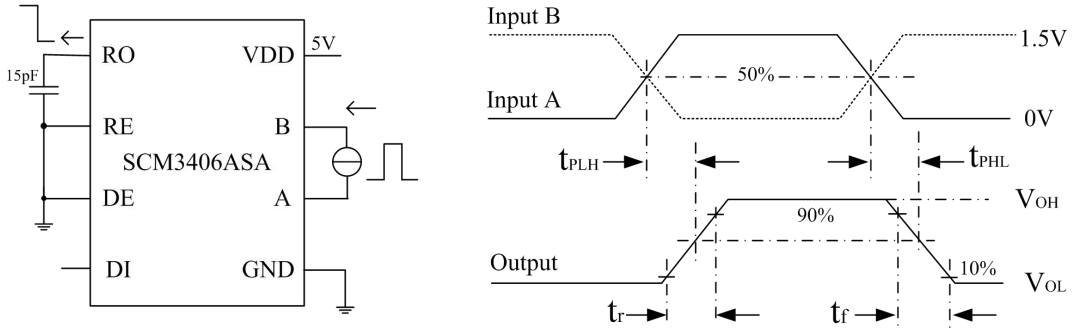

Figure 22 Receiver Switching Test Circuit and Waveforms

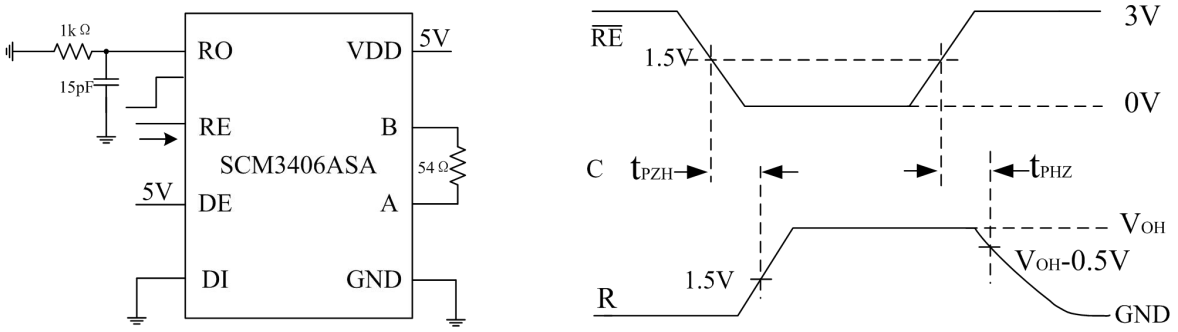

Figure 23 Receiver Enable/Disable Test Circuit and Waveforms, Data Output High

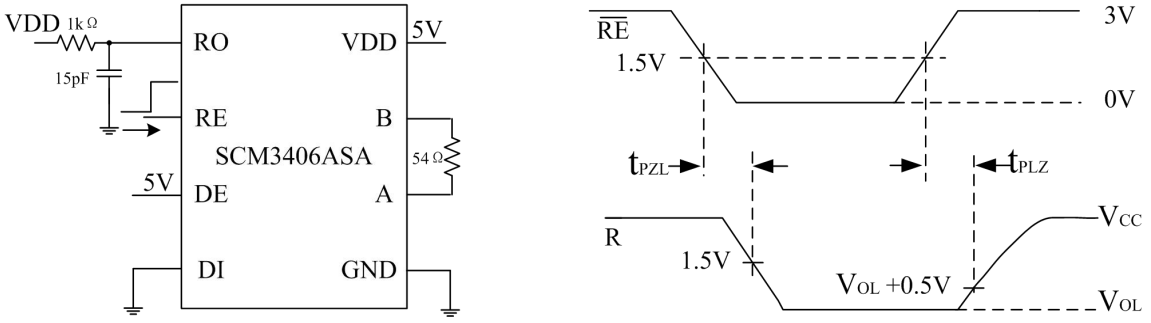

Figure 24 Receiver Enable/Disable Test Circuit and Waveforms, Data Output Low

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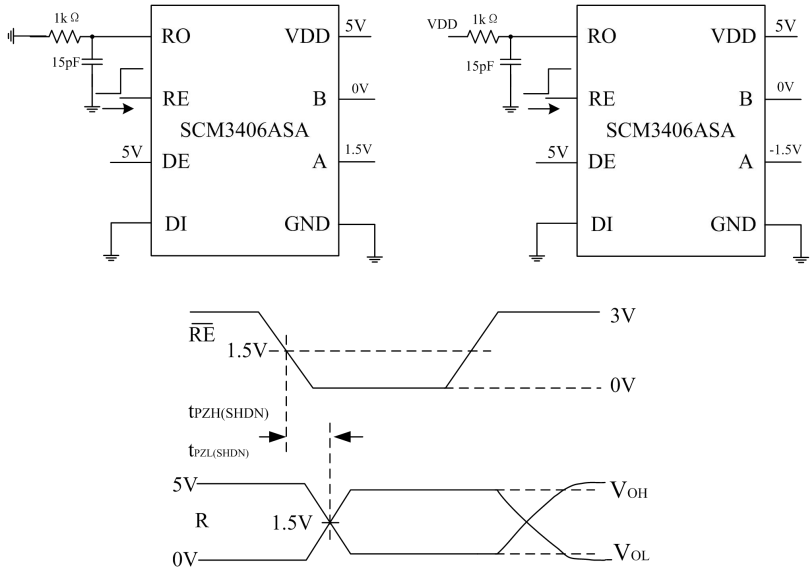

Figure 25 Receiver Enable from Shutdown Test Circuit and Waveforms

Detailed Description

The SCM3406ASA series are advanced RS-485 transceivers. They each contain one driver and one receiver. These devices feature a fail-safe circuitry that guarantees a high receiver output voltage when the receiver inputs are either open, shorted or when they are connected to a terminated transmission line with all drivers disabled. These devices operate with a single 3.0V or 5.0V supply. Drivers limit the output current by over current protection, to avoid the damage to the transceivers.

Receiver input filter: The SCM3406ASA receivers have an integrated input filter which enhances noise immunity of the high-speed differential signals. The receiver propagation delay increases due to this filtering.

Bus fail-safe: Ordinary RS485 bus receivers will be in an indeterminate state when -220mV< A - B <-40mV. This situation can occur whenever the data bus is not being actively driven. The advanced Fail-safe feature of the SCM3406ASA guarantees a high receiver output voltage if the receiver's differential inputs are either shorted, open circuit, or if they are connected to a termination resistor. The SCM3406ASA receiver thresholds are very precise, and the offset between threshold voltage and ground has a margin of at least 40mV.

Load abilities on the bus (256 nodes): The standard receiver input impedance of RS-485 is 12kΩ (1 unit load). A standard RS485 driver can drive at least 32 unit loads. The SCM3406ASA transceiver is design to 1/8th of the standard unit load and the input impedance is higher than 96kΩ, hence allowing up to 256 unit loads, in other words eight times as many. The SCM3406ASA can work combined with other standard RS485 that use the smaller amount of unit loads.

Driver output protection: The device prevents excessive output current caused by fault conditions or driver short circuit. A driver current limit on the output stage provides and ensures immediate protection against short circuits over the entire common mode voltage range.

Expansion Output Design

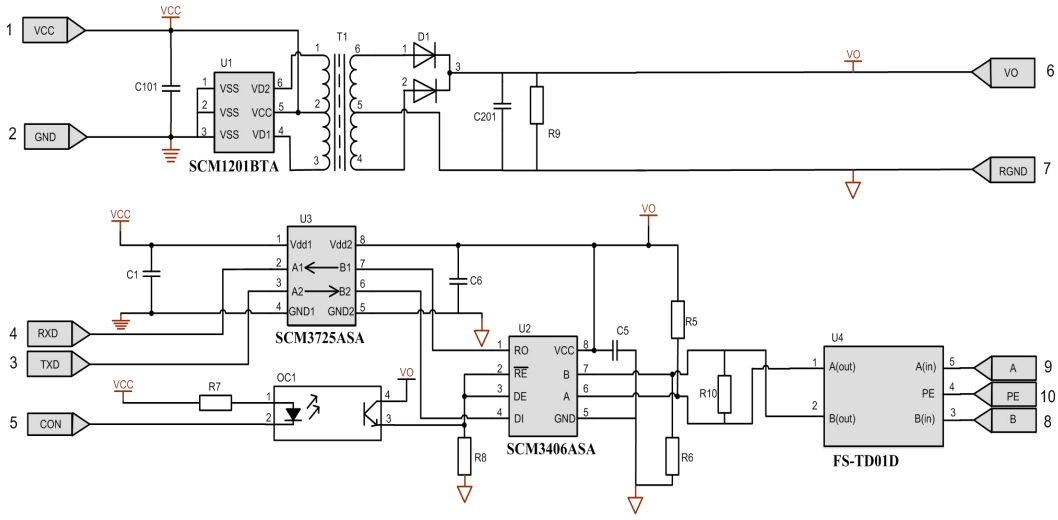

Fig. 26 Schematic diagram of isolation application circuit for UART to RS485 signal

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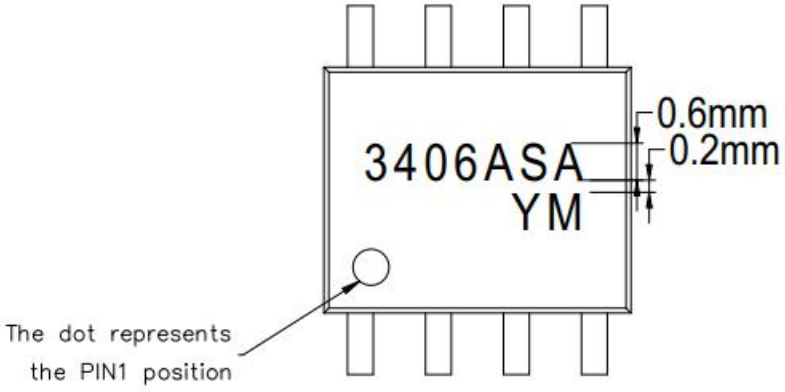
Suggestions for Power Supply

If the input power is a few inches from the SCM3406ASA, as much as possible, connect a 0.1μF bypass capacitor to the VCC pin and a 10μF capacitor near the center tap pin of the transformer.

Ordering Information

Part number	Package	Number of pins	Product Marking	Tape & Reel
SCM3406ASA	SOP	8	3406ASA YM	3k/REEL

Product marking and date code
3406XYZ:
(1) 3406 = Product designation.
(2) X = Version code information (A-Z).
(3) Y = Packaging definition code; S for SOP package,
(4)Z = Operating temperature range (C = 0℃ to +70℃, I =-40℃ to +85℃, A =-40℃ to +125℃, M = -55℃ to +125℃) .
(5) YM = Date code for product traceability; Y = code for production year; M = code for production month.



Note:
1、Typeface: Arial;
2、Character size:
Height: 0.6mm, Spacing: 0.1mm, LineSpacing: 0.2mm;

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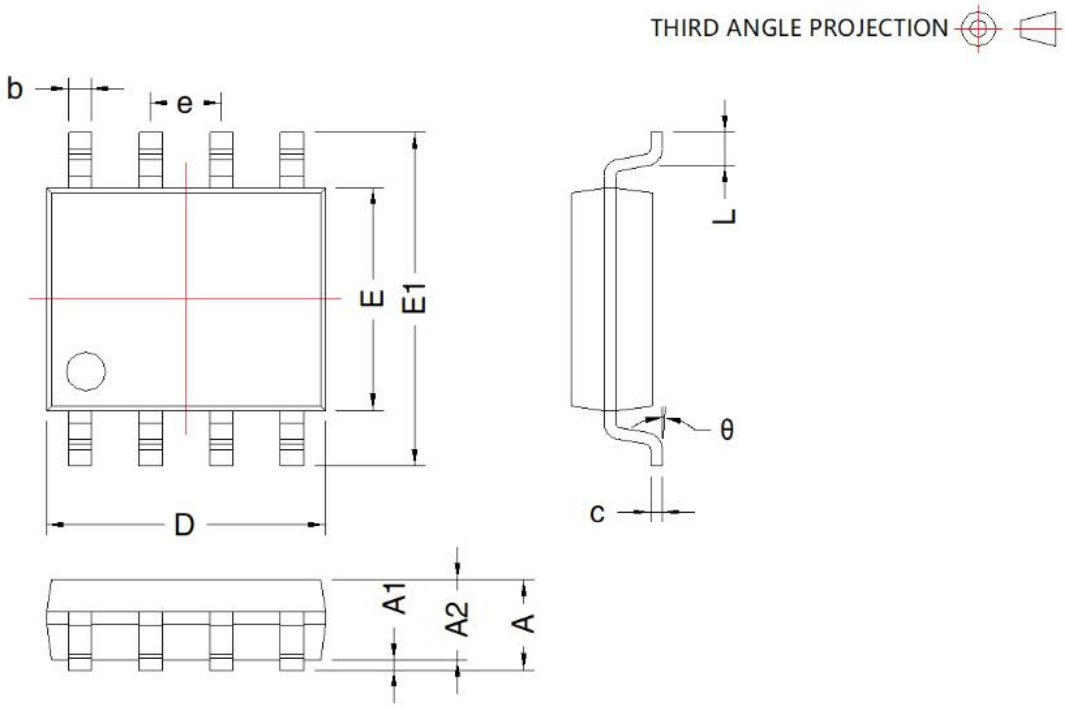

SOP-8				
Mark	Dimension(mm)		Dimension(inch)	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.35	1.55	0.053	0.061
D	4.70	5.10	0.185	0.201
E	3.80	4.00	0.150	0.157
E1	5.80	6.20	0.228	0.244
L	0.40	0.80	0.016	0.031
b	0.33	0.51	0.013	0.020
e	1.27BSC		0.05BSC	
c	0.17	0.25	0.007	0.010
θ	0°	8°	0°	8°

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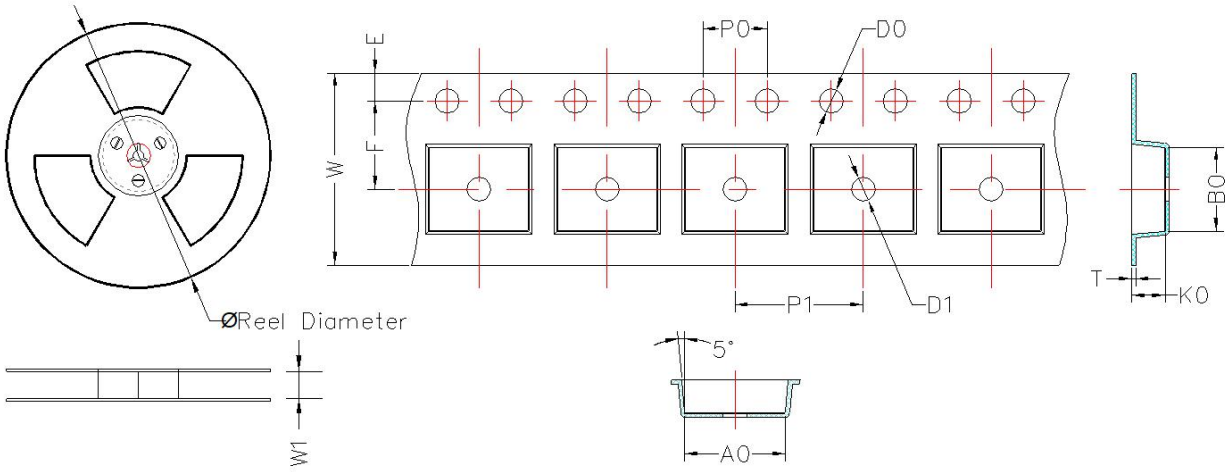
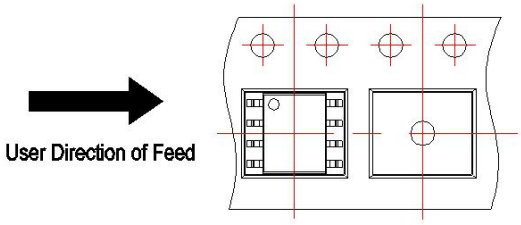


The orientation of IC in tape



Device	Package Type	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	T (mm)	W (mm)	E (mm)	F (mm)	P1 (mm)	P0 (mm)	D0 (mm)	D1 (mm)
SCM3406ASA	SOP-8	3000	330.0	12.4	6.5±0.2	5.45±0.2	2.0±0.2	0.3±0.05	12.0±0.3	1.75±0.1	5.5±0.1	8.0±0.1	4±0.1	1.5±0.1	1.5±0.1

Note: Minimum order quantity is the minimum packing quantity the order quantity is the integer times of MPQ

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